	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	6	(remove or removing or removed) adj10 (impurity or impurities) adj10 (hydrogen adj3 plasma)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/31 11:55
2	BRS	L7	414	diffusing adj3 impurity	USOCR	2002/10/31 13:34
3	BRS	L8	594	(diffus$3) adj10 (impurity or impurities) adj10 resistance	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/31 13:35
4	BRS	L9	14	8 and (thin adj film adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/31 13:55
5	BRS	L10	2875	(contact adj layer) same resistance	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/31 13:58
6	BRS	L11	10	(contact adj layer) same (first adj resistance)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/31 14:08

	Type	L #	Hits	Search Text	DBs	Time Stamp
7	BRS	L12	27	(remove or removing or removed) adj10 (impurity or impurities) same (hydrogen adj3 plasma)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/31 14:24
8	BRS	L13	27	(remov$3) same (impurity or impurities) same (hydrogen) same plasma same (CVD or (chemical adj3 vapor adj3 deposition)) same (anneal or annealing or annealed)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/31 14:33
9	IS&R	L14	1	("6214705").PN.	USPAT	2002/10/31 14:33

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	IS&R	L1	381	(438/149).CCLS.	USPAT	2002/10/31 18:20
2	IS&R	L3	196	(438/482).CCLS.	USPAT	2002/10/31 18:23
3	IS&R	L4	106	(438/156).CCLS.	USPAT	2002/10/31 18:33

DERWENT-ACC-NO: 1996-474266
DERWENT-WEEK: 199843

TITLE: Plasma treatment for semiconductor device mfr. - comprises removing impurity by treating with hydrogen@ and hydrogen chloride or chlorine@ by plasma CVD

PATENT-ASSIGNEE: SEMICONDUCTOR ENERGY LAB[SEME]

PRIORITY-DATA: 1991JP-0169305 (November 28, 1981) , 1996JP-0061890 (November 28, 1981)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2802747 B2	September 24, 1998	N/A	007	H01L 021/205
JP 08241869 A	September 17, 1996	N/A	008	H01L 021/205

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP 2802747B2	Div ex	1991JP-0169305	November 28, 1981
JP 2802747B2	N/A	1996JP-0061890	November 28, 1981
JP 2802747B2	Previous Publ.	JP 8241869	N/A
JP08241869A	Div ex	1991JP-0169305	November 28, 1981
JP08241869A	N/A	1996JP-0061890	November 28, 1981

INT-CL (IPC): C23C014/00; C23C016/50 ; C23F004/00 ; H01L021/205 ; H01L021/3065

RELATED-ACC-NO: 1983-743123;1990-181933 ;1993-055836

ABSTRACTED-PUB-NO: JP08241869A

BASIC-ABSTRACT: The process for treatment comprises removing impurity in a reactive chamber by treating hydrogen and hydrogen chloride or chlorine in a reactive furnace by plasma CVD.

USE - Used in mfg. semiconductor devices.

ADVANTAGE - The device has excellent reproducibility and characteristics.

CHOSEN-DRAWING: Dwg.1/4

TITLE-TERMS:
PLASMA TREAT SEMICONDUCTOR DEVICE MANUFACTURE COMPRISE REMOVE IMPURE TREAT
HYDROGEN@ HYDROGEN CHLORIDE CHLORINE@ PLASMA CVD

DERWENT-CLASS: L03 U11

CPI-CODES: L04-C01B;

EPI-CODES: U11-C03C;

UNLINKED-DERWENT-REGISTRY-NUMBERS: 1532U; 1704U ; 1781U

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C1996-148195
Non-CPI Secondary Accession Numbers: N1996-400122

DERWENT-ACC-NO: 1996-236426
DERWENT-WEEK: 199948

TITLE: Economic refining of highly pure metal - by **removing impurities in metal using single melting process and generating active hydrogen using plasma** arc heating process, while zone melting is conducted

PATENT-ASSIGNEE: ISSHIKI M[ISSHI], MIMURA YM[MIMUI], TACHIBANA RIKO KK[TACHN]

PRIORITY-DATA: 1994JP-0227095 (September 21, 1994)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2960652 B2	October 12, 1999	N/A	007	C22B 009/22
JP 08092662 A	April 9, 1996	N/A	007	C22B 009/00

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP 2960652B2	N/A	1994JP-0227095	September 21, 1994
JP 2960652B2	Previous Publ.	JP 8092662	N/A
JP 08092662A	N/A	1994JP-0227095	September 21, 1994

INT-CL (IPC): C22B009/00; C22B009/20 ; C22B009/22

ABSTRACTED-PUB-NO: JP 08092662A
BASIC-ABSTRACT: The refining of highly pure metal, when impurities included in the metal are removed with a single melting process, comprises employing a plasma arc heating process to generate active hydrogen decomposed under H2-contg. atmos., while zone melting is conducted.

USE - Used to provide a process to conduct refining of highly pure metal.

ADVANTAGE - A more economic refining and retrieval process for highly pure
metal is provided.

CHOSEN-DRAWING: Dwg.1/3

TITLE-TERMS:
ECONOMY REFINE HIGH PURE METAL REMOVE IMPURE METAL SINGLE MELT PROCESS GENERATE
ACTIVE HYDROGEN PLASMA ARC HEAT PROCESS ZONE MELT CONDUCTING

DERWENT-CLASS: M24 M25

CPI-CODES: M24-C; M25-F;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C1996-075469

DOCUMENT-IDENTIFIER: US 20020100908 A1

TITLE: THIN FILM DEVICE PROVIDED WITH COATING FILM, LIQUID CRYSTAL PANEL AND
ELECTRONIC DEVICE, AND METHOD FOR MAKING THE THIN FILM DEVICE

---------- KWIC ---------

[0132] FIG. 4 is a cross-sectional view of a reverse stagger-type amorphous
silicon TFT. An insulating underlayer 32 is formed on a glass substrate 30,
and an amorphous silicon TFT is formed thereon. The insulating underlayer 32
is often omitted. In FIG. 4, a layer or a plurality of layers of gate
insulating films 36 are formed under a gate electrode 34 and a gate line
connected thereto. On the gate electrode 34, an amorphous silicon channel
region 38C is formed, and a source region 38S and a drain region 38D are formed
by diffusing an **impurity into the amorphous silicon**. A pixel electrode 40 is
electrically connected to the drain region 38D through a metal lead layer 42,
and a source line 44 is electrically connected to the source region 38S. The
metal lead layer 42 and the source line are simultaneously formed.

US-PAT-NO: 6468845

DOCUMENT-IDENTIFIER: US 6468845 B1

TITLE: Semiconductor apparatus having conductive thin films and manufacturing apparatus therefor

---------- KWIC ---------

A process ST1 of FIG. 14 will be explained first. Temperature of a semiconductor substrate is controlled, for example, in order to deposit amorphous silicon by vapor-phase reacting disilane Si.sub.2 H.sub.6 and phosphine PH.sub.3 gases. Then, divided amorphous silicon layer 13 is deposited on the surface of the p-type silicon semiconductor substrate 4 on which the silicon oxide film 5 was formed by the gate oxidation at the preceding process, by a CVD or the like, at a film thickness to be deposited at one time film formation not larger than a film thickness prescribed by a critical stress determined according to a fail event. In this case, density of the **impurity phosphorus (P) within the divided amorphous silicon** layers 13 is uniform.

On the surface of a silicon substrate 4, a base film, that is a silicon oxide film, is formed, and amorphous thin films into which an **impurity of a predetermined density has been doped, such as for example amorphous silicon** thin films, are deposited within a range of a film thickness which does not cause an occurrence of fail event, and then the crystallization reaction of the deposited thin films is completed.

DOCUMENT-IDENTIFIER: US 20020126076 A1

TITLE: Liquid crystal display device and method of driving the same

---------- KWIC ---------

[0088] A thin film transistor is fabricated in the island-shaped amorphous silicon film 603. The island-shaped amorphous silicon film 603 is formed on the interlayer insulating film 606 which is formed on the first transparent insulating substrate 605. **Impurity such as phosphorus is doped into the island-shaped amorphous silicon** film 603 by plasma-enhanced chemical vapor deposition (CVD), for instance, to thereby form source and drain regions. The signal line 604 is electrically connected to the drain region, and the pixel electrode 600 is electrically connected to the source region.

US-PAT-NO: 6214705

DOCUMENT-IDENTIFIER: US 6214705 B1

TITLE: Method for fabricating a gate eletrode

---------- KWIC ---------

In addition to the second amorphous silicon layers 124, the doped amorphous
silicon layers are formed by, for example, chemical vapor deposition (CVD) and
a dopant such as phosphorus is simultaneously in-situ doped thereinto. The
dopant concentration is about 1.times.10.sup.19 to 1.times.10.sup.22
atom/cm.sup.3. By doping only even-numbered layers in a plurality of amorphous
silicon layers, such as the layers 124, 128, . . . 132 in this embodiment, an
**impurity distribution more uniform than that of a single doped amorphous
silicon** layer is achieved after performing an annealing step. The uniform
distribution is helpful to lower the resistance of the gate electrode.